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1. **An elastic pipeline mechanism by self-timed circuits**
   Komori, S.; Takata, H.; Tamura, T.; Asai, F.; Ohno, T.; Tomisawa, O.; Yamasaki, T.; Shima, K.; Asada, K.; Terada,
   Solid-State Circuits, IEEE Journal of
   Volume 23, Issue 1, Feb. 1988 Page(s):111 - 117
   IEEE JNL

2. **A 40-MFLOPS 32-bit floating-point processor with elastic pipeline scheme**
   Komori, S.; Takata, H.; Tamura, T.; Asai, F.; Ohno, T.; Tomisawa, O.; Yamasaki, T.; Shima, K.; Nishikawa, H.; Terada, H.;
   Solid-State Circuits, IEEE Journal of
   Volume 24, Issue 5, Oct 1989 Page(s):1341 - 1347
   IEEE JNL

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